AMENDMENTS TO THE CLAIMS

Claims 1-16 (Cancelled)

17. (Currently amended) The method of Claim 32, wherein the FPGA Is programmed to perform steps including:

receiving the real and imaginary inputs at first and second inputs of an FFT block via a pair of gateway in blocks;

coupling an output of a double delay block to a third input of the FFT block, the third input being adapted to mark data input as valid or invalid;

coupling an output of a k=0 block to a fourth input of the FFT block, the fourth input being adapted to control a forward or a reverse transform;

coupling outputs of the FFT block to at least one D flip flop-based registers adapted to provide a signal latency; and

coupling the outputs of the registers to at least one gateway out.

Claims 18-30 (Cancelled)

31. (Currently amended) A method of performing a numerical simulation with a Field Programmable Gate Array (FPGA) and a separate central processing unit (CPU) ~~CPU and an FPGA~~, the method comprising:

using the CPU to perform a numerical simulation including generating input signals and sending the input signals to the FPGA;

using the FPGA to apply a model to the input signals and send results of the model back to the CPU, the FPGA also generating a first output that marks data as valid or invalid, a second output that indicates the first sample of each frame, and a third output that indicates when the model can accept data; and

wherein the CPU uses the results in the numerical simulation and the outputs to maintain data flow with the FPGA.

32. (Currently amended) The method of claim 31, wherein the input signals include sine wave functions representing real and imaginary inputs; and wherein the model includes a [[FFT]] Fast Fourier Transform (FFT).

33. (Previously presented) The method of claim 32, wherein the FPGA converts the real and imaginary inputs from double point precision to fixed point prior to performing the transform; and wherein the FPGA converts the results of the FFT from fixed point back to double precision prior to sending the results back to the CPU.

34. (Previously presented) The method of claim 32, wherein the CPU performs a numerical simulation of a radar system.

35. (Currently amended) Apparatus comprising [[:]] a central processing unit (CPU) and a Field Programmable Gate Array (FPGA) for performing different portions of a numerical simulation;

[[a]] the CPU programmed to perform a numerical simulation of sine wave functions representing real and imaginary inputs; [[and]]

[[an]] the FPGA programmed to perform [[an]] a Fast Fourier Transform (FFT) [[FFT]] on the inputs and send results of the FFT back to the CPU, the FPGA also generating a first output that marks data as valid or invalid, a second output that indicates the first sample of each frame, and a third output that indicates when the FFT can accept data; [[and]]

the CPU using the results in the numerical simulation and the outputs to maintain data flow with the FPGA.

36. (Previously presented) The apparatus of claim 35, wherein the FPGA converts the real and imaginary inputs from double point precision to fixed point prior to performing the transform; and wherein the FPGA converts the results of the FFT from fixed point back to double precision prior to sending the results back to the CPU.

37. (Previously presented) The apparatus of claim 35, wherein the CPU performs a numerical simulation of a radar system.